Claims 1-2 (canceled)

3. (currently amended) The circuit of claim 25~~claim 2~~, wherein outputs of the first and second peak detectors are combined to provide a peak detection signal to the control circuitry.

4. (original) The circuit of claim 3, wherein the first and second peak detectors are matched.

5. (original) The circuit of claim 3, wherein the outputs of the first and second peak detectors are combined by subtracting the output of the second peak detector from the output of the first peak detector.

6. (original) The circuit of claim 3, further comprising a divider circuit coupled between the first peak detector and the output of the power amplifier.

7. (previously presented) The circuit of claim 6, wherein the divider is comprised of a first and second capacitor coupled between the output of the power amplifier and ground.

8. (previously presented) The circuit of claim 25, further comprising a power detector coupled to the output of the power amplifier and to the control circuitry for detecting the output power of the power amplifier.

Claims 9-10 (canceled)

11. (previously presented) The circuit of claim 32, wherein the first peak detector is coupled to the output of the power amplifier and the second peak detector is coupled to a reference tone.

12. (original) The circuit of claim 11, wherein the first and second peak detectors are matched.

13. (previously presented) The circuit of claim 32, further comprising a power detector coupled to the output of the power amplifier and to the power control circuitry for detecting the output power of the power amplifier.

Claims 14-24 (canceled)

25. (currently amended) A circuit for protecting devices in an RF power amplifier comprising:

a power detector coupled to the output of the RF power amplifier for detecting the output power of the RF power amplifier;

a peak detector coupled to one or more critical nodes in the RF power amplifier for detecting peak voltages at the one or more critical nodes, wherein the peak detector further comprises a first peak detector having an input coupled to the one or more critical nodes in the RF power amplifier, and a second peak detector having an input coupled to a reference tone;

a divider circuit coupled between the peak detector and the one or more critical nodes; and

power control circuitry coupled to the power detector and to the peak detector for controlling the output power of the power amplifier, wherein the power control circuitry protects devices in the RF power amplifier by decreasing the gain of the power amplifier when the peak

detector detects a voltage above a voltage threshold at the one or more critical nodes in the RF power amplifier.

26. (previously presented) The circuit of claim 25, wherein the peak detector detects peak voltages present across one or more transistors in the RF power amplifier.

27. (previously presented) The circuit of claim 25, wherein the peak detector detects peak voltages present across one or more switching devices in the RF power amplifier.

28. (previously presented) The circuit of claim 25, wherein the one or more critical nodes do not include the output of the power amplifier.

Claim 29 (canceled)

30. (previously presented) The circuit of claim 25, wherein the divider circuit is a capacitive divider circuit.

31. (previously presented) The circuit of claim 25, wherein the divider circuit divides the voltage detected at the one or more critical nodes; and wherein the input of the peak detector is coupled to the divided voltage.

32. (previously presented) A circuit comprising:

an RF power amplifier having an input and an output;

a power detector coupled to the output of the RF power amplifier for detecting the output power of the RF power amplifier;

a peak detector coupled to the power amplifier for detecting a peak voltage at a node of the power amplifier, wherein the node is a node other than the output of the power amplifier, wherein the peak detector is comprised of first and second matched peak detectors; and

power control circuitry coupled to the peak detector and to the power amplifier for controlling the gain of the power amplifier, wherein the power control circuitry limits the power at the output of the power amplifier when the peak detector detects a peak voltage greater than a threshold voltage.

33. (previously presented) The circuit of claim 32, further comprising a divider circuit coupled between the peak detector and the node of the power amplifier.

34. (previously presented) A circuit for protecting devices in an RF power amplifier comprising:

a power detector coupled to the output of the RF power amplifier for detecting the output power of the RF power amplifier;

a peak detector coupled to one or more critical nodes in the RF power amplifier for detecting peak voltages at the one or more critical nodes, wherein the peak detector further comprises a first peak detector having an input coupled to the one or more critical nodes in the RF power amplifier, and a second peak detector having an input coupled to a reference tone; and

power control circuitry coupled to the power detector and to the peak detector for controlling the output power of the power amplifier, wherein the power control circuitry protects devices in the RF power amplifier by decreasing the gain of the power amplifier when the peak

detector detects a voltage above a voltage threshold at the one or more critical nodes in the RF power amplifier.

35. (previously presented) The circuit of claim 34, wherein outputs of the first and second peak detectors are combined to provide a peak detection signal to the control circuitry.

36. (previously presented) The circuit of claim 35, wherein the first and second peak detectors are matched.

37. (previously presented) The circuit of claim 35, wherein the outputs of the first and second peak detectors are combined by subtracting the output of the second peak detector from the output of the first peak detector.

38. (previously presented) The circuit of claim 35, further comprising a divider circuit coupled between the first peak detector and the output of the power amplifier.

39. (previously presented) The circuit of claim 38, wherein the divider is comprised of a first and second capacitor coupled between the output of the power amplifier and ground.